

FIG. 1 (PRIOR ART)

I1(branch Loop)  
I2  
I3(Not in Cache  
Memory)  
•  
•  
Loop I10  
I11  
I12

	C1	C2	C3	C4	C5	C6	C7	C8	
Fetch	I1	I2	I3	I3	I3	I10	I11	I12	
Decode		I1	I2	I2	I2	I2	I10	I11	
Execute			I1	I1	I1	I1	I2	I10	

FIG. 2B

FIG. 2A

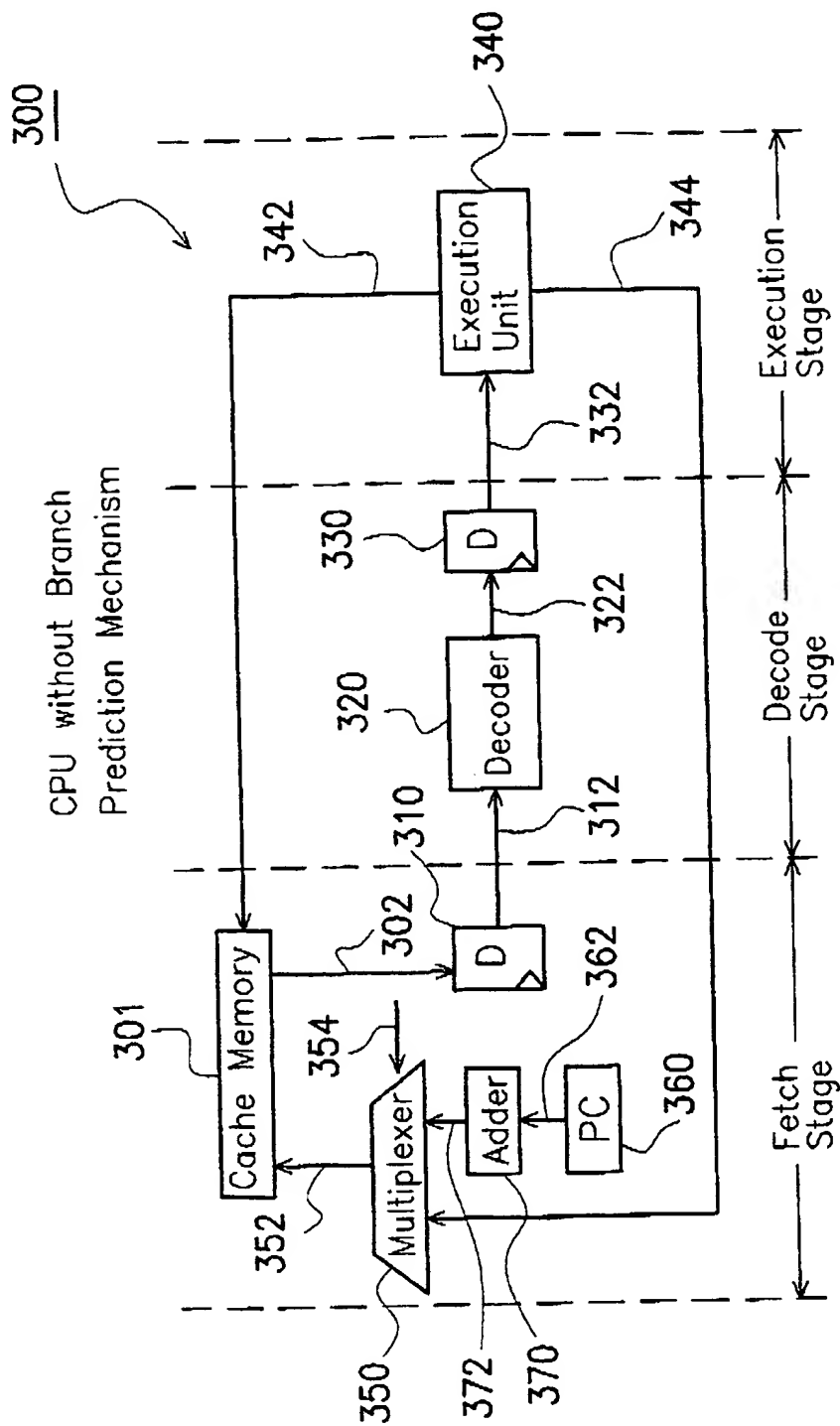


FIG. 3

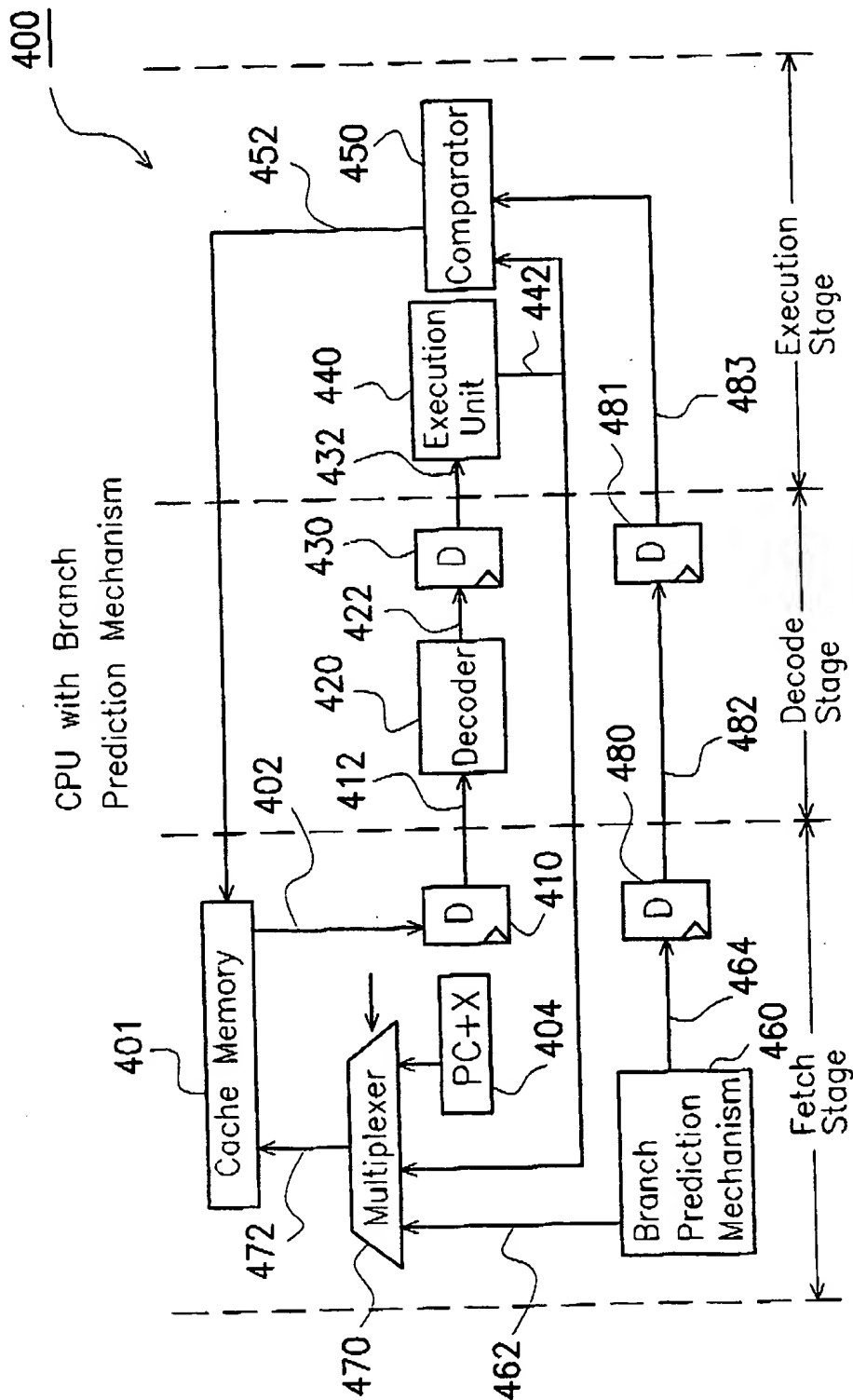


FIG. 4

	C1	C2	C3	C4	C5	C6	
Fetch	I1	I2	I3	I10	I11	I12	
Decode		I1	I2	I3	I10	I11	
Execute			I1	I2	I3	I10	

FIG. 5